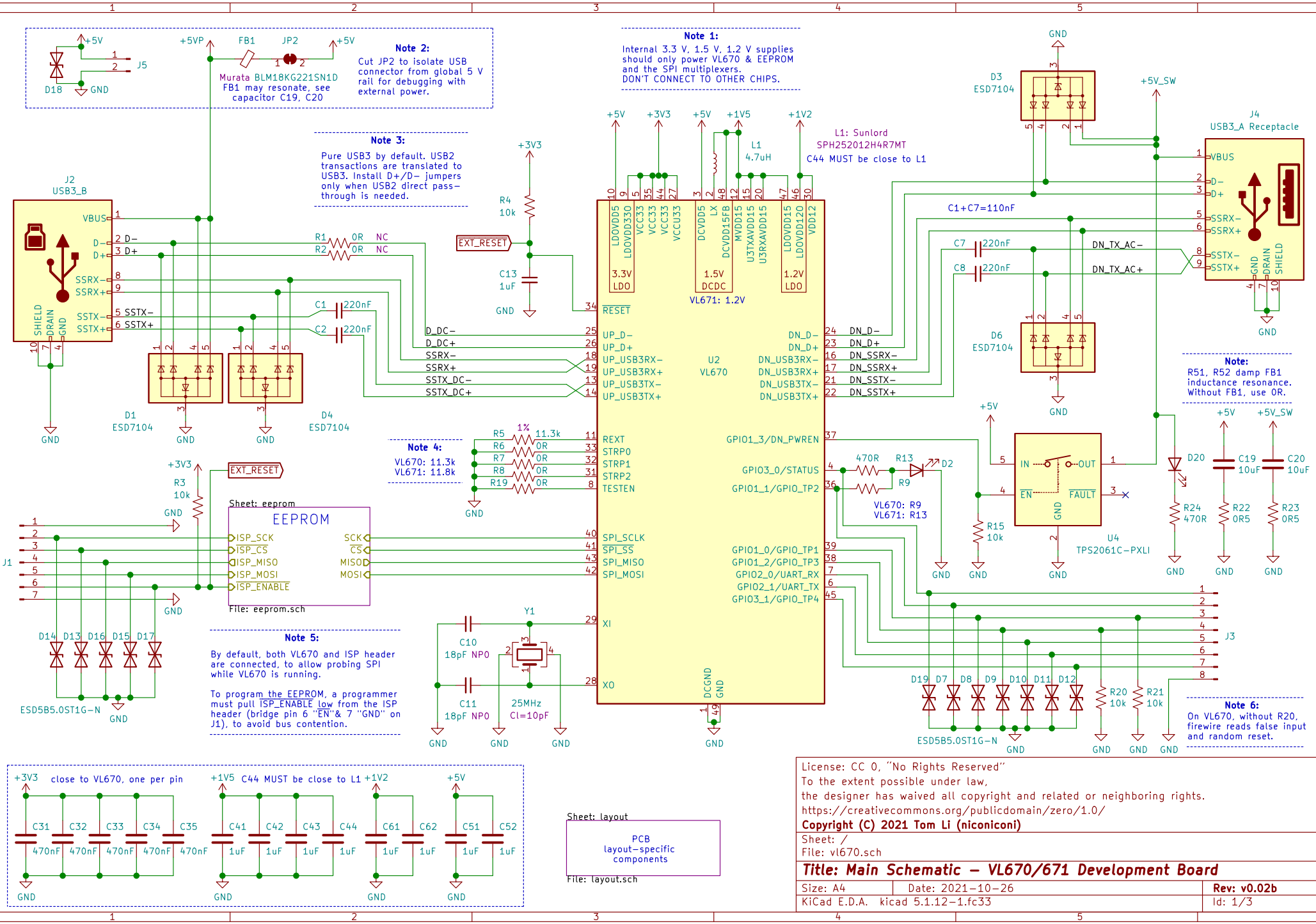
Note 1:
Internal 3.3 V, 1.5 V, 1.2 V supplies should only power VL670 & EEPROM and the SPI multiplexers.
DON'T CONNECT TO OTHER CHIPS.
Note 2:
Cut JP2 to isolate USB connector from global 5 V rail for debugging with external power.
Murata BLM18KG221SN1D
FB1 may resonate, see capacitor C19, C20
Note 3:
Pure USB3 by default. USB2 transactions are translated to USB3. Install D+/D− jumpers only when USB2 direct pass-through is needed.
L1: Sunlord SPH252012H4R7MT
C44 MUST be close to L1
L1 4.7uH
C1+C7=110nF
Note:
R51, R52 damp FB1 inductance resonance.
Without FB1, use 0R.
Note 4:
VL670: 11.3k
VL671: 11.8k
VL670: R9
VL671: R13
Note 5:
By default, both VL670 and ISP header are connected, to allow probing SPI while VL670 is running.
To program the EEPROM, a programmer must pull ISP_ENABLE low from the ISP header (bridge pin 6 "EN" & 7 "GND" on J1), to avoid bus contention.
Note 6:
On VL670, without R20, firewire reads false input and random reset.
VL671: 1.2V
U2
VL670
U4
TPS2061C-PXLI
Sheet: eeprom
EEPROM
File: eeprom.sch
Sheet: layout
PCB layout-specific components
File: layout.sch
close to VL670, one per pin
C44 MUST be close to L1
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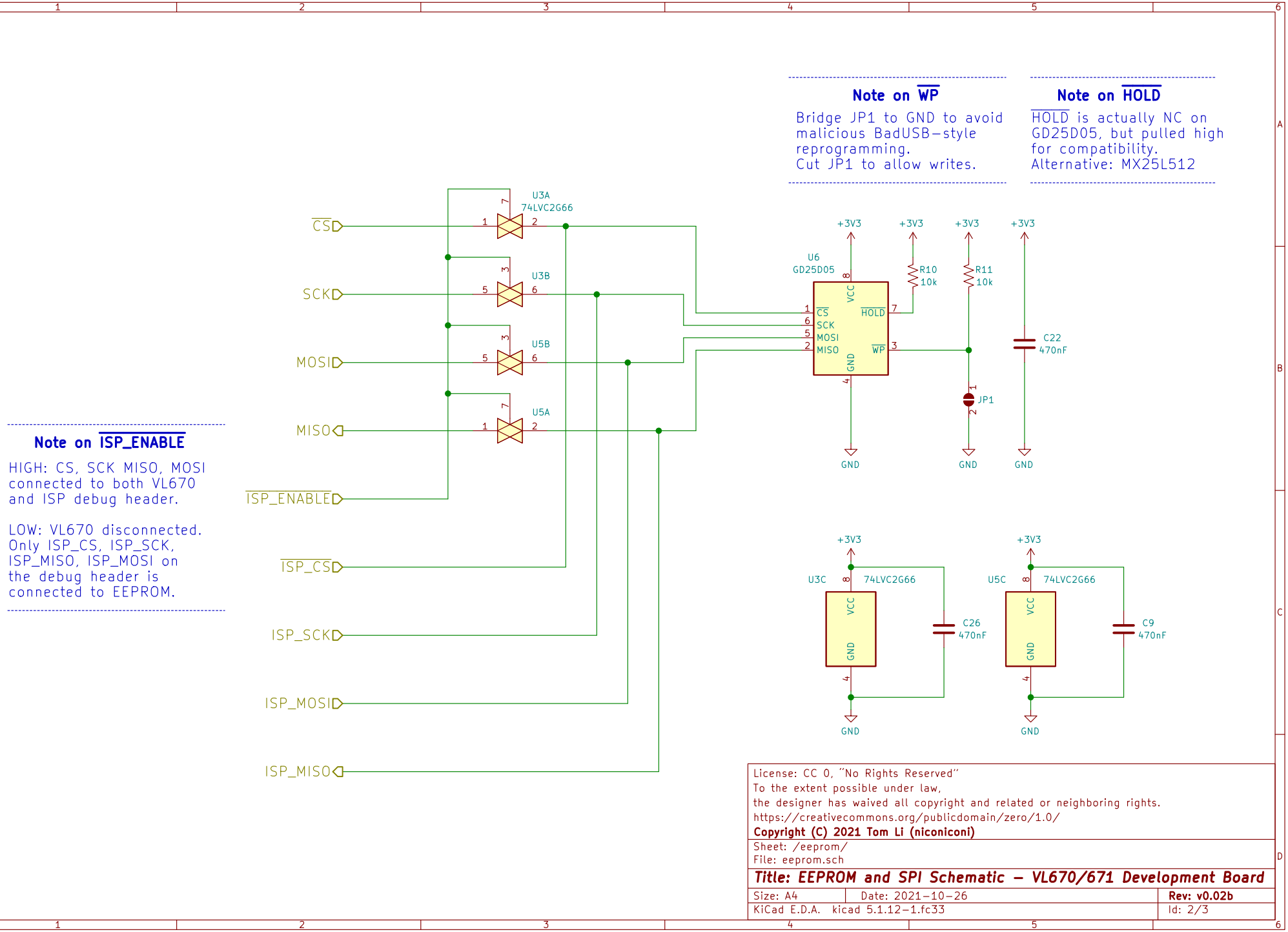
Sheet: /
File: vl670.sch
Title: Main Schematic – VL670/671 Development Board
Size: A4
Date: 2021-10-26
Rev: v0.02b
KiCad E.D.A. kicad 5.1.12-1.fc33
Id: 1/3


Note on WP
Bridge JP1 to GND to avoid malicious BadUSB−style reprogramming.
Cut JP1 to allow writes.
Note on HOLD
HOLD is actually NC on GD25D05, but pulled high for compatibility.
Alternative: MX25L512
Note on ISP_ENABLE
HIGH: CS, SCK MISO, MOSI connected to both VL670 and ISP debug header.
LOW: VL670 disconnected. Only ISP_CS, ISP_SCK, ISP_MISO, ISP_MOSI on the debug header is connected to EEPROM.
U3A
74LVC2G66
U3B
U5B
U5A
CS
SCK
MOSI
MISO
ISP_ENABLE
ISP_CS
ISP_SCK
ISP_MOSI
ISP_MISO
U6
GD25D05
+3V3
R10
10k
R11
10k
C22
470nF
JP1
GND
U3C
U5C
C26
C9
470nF
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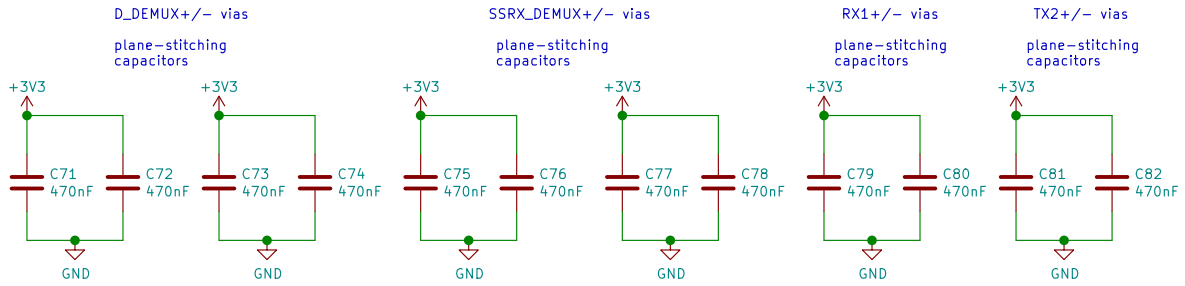
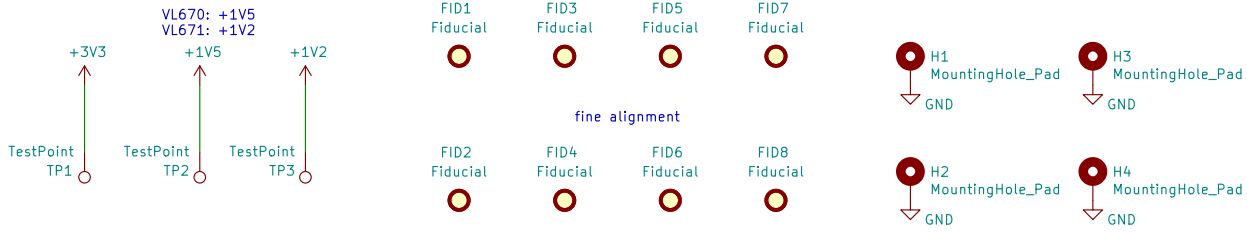
Sheet: /eeprom/
File: eeprom.sch
Title: EEPROM and SPI Schematic – VL670/671 Development Board
Size: A4
Date: 2021−10−26
Rev: v0.02b
KiCad E.D.A. kicad 5.1.12−1.fc33
Id: 2/3





Sheet: /layout/
File: layout.sch

Title: PCB-specific Schematic – VL670/671 Development Board

Size: A4	Date: 2021-10-26	**Rev: v0.02b**
KiCad E.D.A. kicad 5.1.12-1.fc33		Id: 3/3